REMARKS

I. STATUS OF CLAIMS

In accordance with 37 C.F.R. § 1.173(c), the status of the claims are as follows:

Claims 1-33 and 40-54 are pending in the reissue application.

Claims 1-33 are original claims and remain allowed. No changes have been made to claims 1-33.

Claims 34-54 were previously added in the preliminary amendment filed November 24, 2003, with claims 34-39 being canceled in the amendment filed November 20, 2006.

Claims 40 and 47 are being amended in the enclosed amendment.

No new matter has been added.

II. EXPLANATION OF SUPPORT IN DISCLOSURE FOR AMENDMENTS

Claims 40 and 47 have been amended as follows: "wherein the total bit width of the instruction bus is shorter than M * N bits." The amendment is intended to clarify the meaning of "bit width" as explained below in the prior art discussion. Same as for the previous amendment, support for the aforementioned feature of the present invention can be found, for example, in Figures 4, 7 and 11 of Applicants' drawings and the corresponding disclosure in Applicants' specification. For example, one exemplary embodiment is shown in Figure 4 (illustrating relationship between instruction register 23 which is a part of the instruction supplying/issuing unit 20 and decoding unit 30) with corresponding disclosure at col. 9, lines 11-15 of parent USP No. 6,324,639. Specifically, the specification discloses that the "the instruction register 23 is composed of four 21-bit registers and stores the four units that are transferred from the instruction buffer 22 [whereby the] instruction register 23 issues up to four of these units to the

decoding unit 30." Accordingly, as configured in this exemplary embodiment, the bus width would be 84 bits which is shorter than M * N (noting that M is 42 bits for the maximum two-unit instruction while N is 3 for the three decoders 33-35).

III. PRIOR ART REJECTION

Claims 40-54 stand rejected under 35 U.S.C. § 102 as being anticipated by Eickemeyer et al. '746 ("Eickemeyer"). Claims 40 and 47 are independent. This rejection is respectfully traversed for the following reasons.

Claims 40 and 47 each embody an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the total bit width of the instruction bus is shorter than M * N bits; where M is the maximum bit length of an instruction that can be executed in parallel and N is the number of instructions that can be executed in parallel. In direct contrast, Eickemeyer expressly discloses (col. 12, lines 5-14):

> the rule for compounding a set of instructions which includes variable instruction lengths provides that all instructions which are 2 bytes or 4 bytes long are compoundable with each other. That is, ... a 4 byte instruction is capable of parallel execution with another 2 byte ***or another 4 byte instruction***. The rule further provides that all instructions which are 6 bytes long are not compoundable. (emphasis added)

Accordingly, Eickemeyer discloses only a conventional bus configuration having a bus width which is sufficient to handle processing the maximum bit size.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Pan. Applicants and Applicants' representative would like to thank Examiner Pan for his courtesy in conducting the interview and for his assistance in resolving issues. As a result of the interview, it was agreed that the enclosed amendment would appear to obviate the Examiner's broad interpretation of the claimed "bit width of the instruction bus."

Specifically, the Examiner alleged that the "bit width of the instruction bus" could be interpreted based on bit width ***actually used at a given point in time***. To read Eickemeyer onto the claims, the Examiner therefore relied on the condition in which the instruction bus of Eickemeyer is not accessed for its entire width (e.g., when a 2 bit and 4 bit instruction are processed), as the bit width of the instruction bus being shorter than M * N bits. In order to obviate this interpretation, the term "total" has been included in claims 40 and 47 to qualify "bit width." Because Eickemeyer expressly discloses that a 4 "bit" instruction is capable of parallel execution with another 4 bit instruction, the ***total*** bit width of the instruction bus of Eickemeyer must be at least 8 bits to accommodate the two 4 "bit" instructions. Accordingly, the total bit width of the instruction bus in Eickemeyer is at least equal to (M * N) 4 * 2 = 8 bits so as to accommodate the expressly disclosed capability of having two 4 bit instructions processed in parallel, so that the total bit width of the instruction bus in Eickemeyer is NOT shorter than M * N bits.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Eickemeyer does not anticipate claims 40 and 47, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 40 and 47 are patentable for the

reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

III. CONCLUSION

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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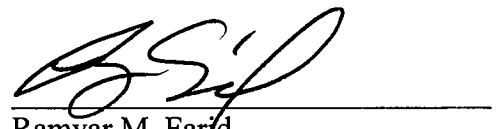

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